Code No: 5455AF

R17

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech I Semester Examinations, June/July - 2018
CPLD AND FPGA ARCHITECTURES AND APPLICATIONS
(Embedded Systems)

Time: 3hrs **Max.Marks:75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

5 × 5 Marks = 25

1.a) Discuss the design of PAL with an example. [5]
b) Explain the different programming technologies of FPGA. [5]
c) Explain programmable routing matrix of Xilinx XC2000 series. [5]
d) Explain, how the ACT3 architecture is different from ACT1 architecture? [5]
e) Explain the general design issues in designing logic circuits using ACT devices. [5]

PART - B

5 × 10 Marks = 50

2. Compare ROM, PAL and PAL with respect to all features, programming aspects and applications. [10]

OR

3. Design a Parallel Adder circuit with Accumulation using CPLD. [10]

4. Explain the general block diagram of FPGA with neat sketches. [10]

OR

5. Draw and explain different design stages involved in the FPGA design flow. [10]

6. Explain the architecture of XC3000 FPGA with neat sketches. [10]

OR

7. Draw the schematic diagram of Xilinx based XC 4000 CLB and describes its functional operation in detail. [10]

8. Explain the architecture of ACT2 FPGA with neat diagrams. [10]

OR

9. Explain the routing architecture of ACT2, ACT1 FPGA's in detail. [10]

10. Design a fast video controller with any ACT device. [10]

OR

11. Explain the implementation of fast DMA controller with any ACT device. [10]

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