Code No: 5455AG

R17

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations, June/July - 2018

DIGITAL SYSTEM DESIGN

(Embedded Systems)

Time: 3hrs **Max.Marks:75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

5 × 5 Marks = 25

1.a) What are static hazards and how it can be eliminated? [5]
b) Explain with an example about BCD adders. [5]
c) Discuss about state machine charts. [5]
d) Define fault detection and redundancy. [5]
e) Write about bridging faults. [5]

PART - B

5 × 10 Marks = 50

2.a) Find a circuit that has no static hazards and implements the Boolean function $F(A, B, C, D)=\sum(0, 2, 6, 7, 8, 10, 12)$
b) With respect to an asynchronous sequential machine, explain about minimal closed corners. [5+5]

OR

3.a) Explain about the finding a minimal cover using a prime-implicant table.
b) The response of the machine shown in table 1 below to an un known input sequence is give to the experimenter. Devise a procedure that the experimenter may use in order to identify the initial state. What are the minimum-length sequences that will make such an identification possible? [5+5]

Table 1

PS	NS	
	$x = 0$	$x = 1$
A	A, 0	B, 0
B	C, 0	D, 0
C	D. 1	C. 1
D	B. 1	A.1

4.a) With the help of neat block diagram, explain working of iterative n-bit comparator.

b) With necessary timing diagram, state machine and state table, explain steps for analyzing clocked synchronous state machines. [4+6]

OR

5.a) Realize full-adder using 3-8 line decoder and two NOR gates.

b) Design 8-bit priority encoder using PAL20L8 PLD device. [5+5]

6. Obtain the SM charts for multiplier controller and realize it using flip flop and combinational circuit. [10]

OR

7. Draw the ASM chart to detect the overlapping sequence 1010 from the incoming bit stream and output 1 for each detection.
Ex: x: 10101010110- - - - - - -
Z: 00010101000- - - - - -
Implement the controller circuit using MUX method. [10]

8. With the help of an example, explain PODEM algorithm. [10]

OR

9. What is the significance of Kohavi Algorithm? Explain how it detects multiple faults in a two-level networks with a simple example. [10]

10. Explain the need of logical fault models in digital circuit testing. Discuss in detail, the single stuck-at fault models and bridging fault models. [10]

OR

11.a) What is the significance of Fault collapsing? Explain the fault collapsing in EX-OR circuit.

b) Describe briefly the various DFT Schemes used in digital circuits. [5+5]

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