6.012 Microelectronic Devices and Circuits
Spring 2007

April 25, 2007
Quiz #2

	Problem #points
NAME_____	1_____
RECITATION TIME_____	2_____
	3_____
	Total_____

General guidelines (please read carefully before starting):

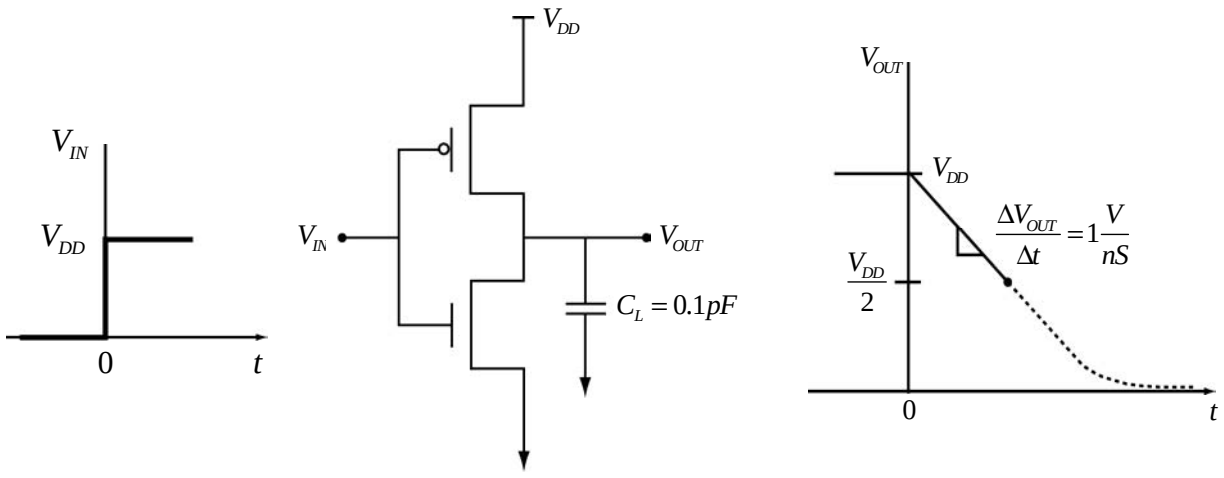
- Make sure to write your name on the space provided above.
- Open book: you can use any material you wish. But no computers.
- All answers should be given in the space provided. Please do not turn in any extra material.
- You have 120 minutes to complete the quiz.
- Make reasonable approximations and *state them*, i.e. low-level injection, extrinsic semiconductor, quasi-neutrality, etc.
- Partial credit will be given for setting up problems without calculations. NO credit will be given for answers without reasons.
- Use the symbols utilized in class for the various physical parameters, i.e. N_a, τ, ε, etc.
- Pay attention to problems in which *numerical answers* are expected. An algebraic answer will not accrue full points. Every numerical answer must have the proper *units* next to it. Points will be subtracted for answers without units or with wrong units. In situations with a defined axis, the *sign* of the result is also part of the answer.

Unless otherwise stated, use:

$q = 1.6 \times 10^{-19}$ C
$kT/q = 25$ mV at room temperature
$n_i = 10^{10}$ cm^{-3} for silicon at room temperature
$\varepsilon_{si} = 10^{-12}$ F/cm $\varepsilon_{ox} = 3.45 \times 10^{-13}$ F/cm

1. (30 points)

You are given a CMOS inverter with a step input voltage from 0 to V_{DD} at $t = 0$, resulting in an output voltage V_{OUT} vs. t shown below. The load capacitance $C_L = 0.1pF$ accounts for all load capacitance components.



(a) Given $V_{DD} = 1.5V$ and that the devices are sized such that $V_M = \frac{V_{DD}}{2}$, calculate t_{pHL} .

(b) Calculate the current I_{Dn} at $0 < t < t_{pHL}$.

(c) Given $V_{Tn} = 0.5V$ and $\mu_n C_{ox} = \frac{50\mu A}{V^2}$, find $\frac{W}{L}$ of the NMOS transistor.

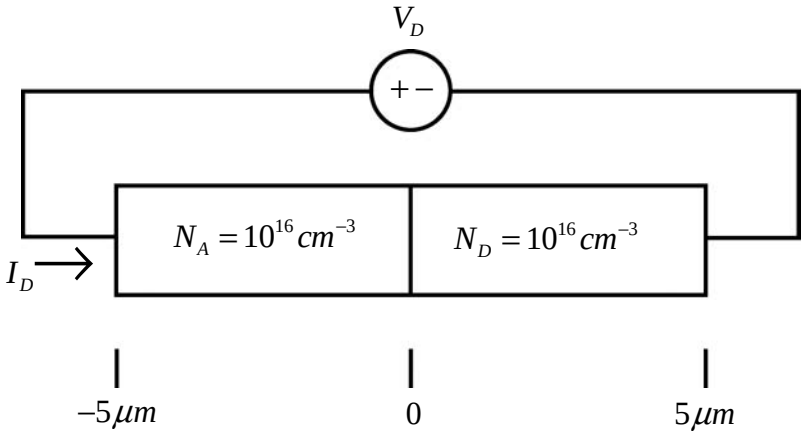
For parts (d) and (e) assume $V_{DD} = 2.5V$.

(d) Calculate the new slope of the output voltage $\frac{\Delta V_{OUT}}{\Delta t}$, at $0 < t < t_{pHL}$.

(e) Calculate the new t_{pHL} .

2. (35 points)

You are given a p-n junction diode that is conducting a current I_D equal to $2\mu A$ when a voltage, V_D, is applied. Assume no generation or recombination inside the diode, and ignore the space charge region width in your calculations for this problem.



Diode parameters

$D_n = 20 cm^2 / \sec$

$D_p = 10 cm^2 / \sec$

Area $2x10^{-6} cm^2$

(a) Calculate the minority carrier concentrations $n_p(0), p_n(0)$.

(b) Calculate V_D.

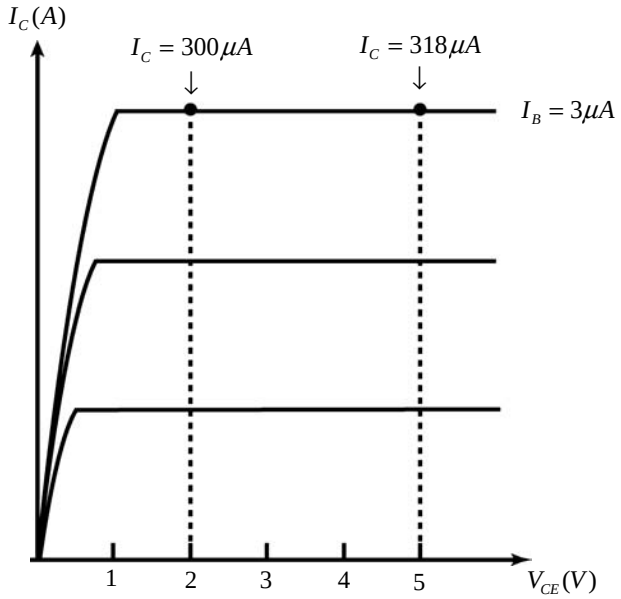
(c) What is the total **majority** carrier current on the n-side of the diode?

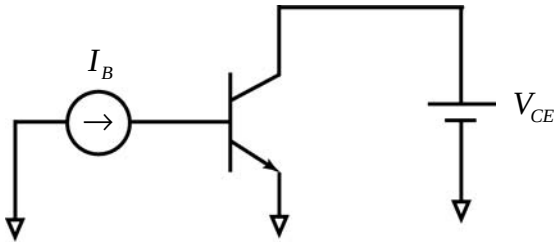
(d) Calculate the **majority** carrier diffusion current on the n-side of the diode. Hint: Quasi neutrality implies $n_n(x) = p_n(x)$.

(e) Calculate the electric field in the quasi-neutral region on the n-side of the diode.

3. (35 points)

An npn bipolar transistor has $D_n = 25cm^2/s$ and $D_p = 12.5cm^2/s$. The common emitter output characteristics are as follows:





(a) Find the transconductance, g_m, at $V_{CE} = 2V, I_B = 3\mu A$.

(b) Find the input resistance, r_π, at $V_{CE} = 2V, I_B = 3\mu A$.

(c) Find the output resistance, r_o, at $V_{CE} = 2V, I_B = 3\mu A$.

(d) Given the input capacitance, $C_\pi = 0.2\,pF$ at $V_{CE} = 2V, I_B = 3\mu A$, estimate the width of the quasi-neutral base region. Neglect the capacitance due to the emitter-base space charge region.

(e) Estimate the number of excess minority electrons in the base under the same bias conditions as in (d) above.

(f) If the quasi-neutral base width is reduced by a factor of two, calculate the number of excess electrons in the base under the same bias conditions as in (e) above.

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