Lecture 12
Digital Circuits (II)
MOS INVERTER CIRCUITS

Outline

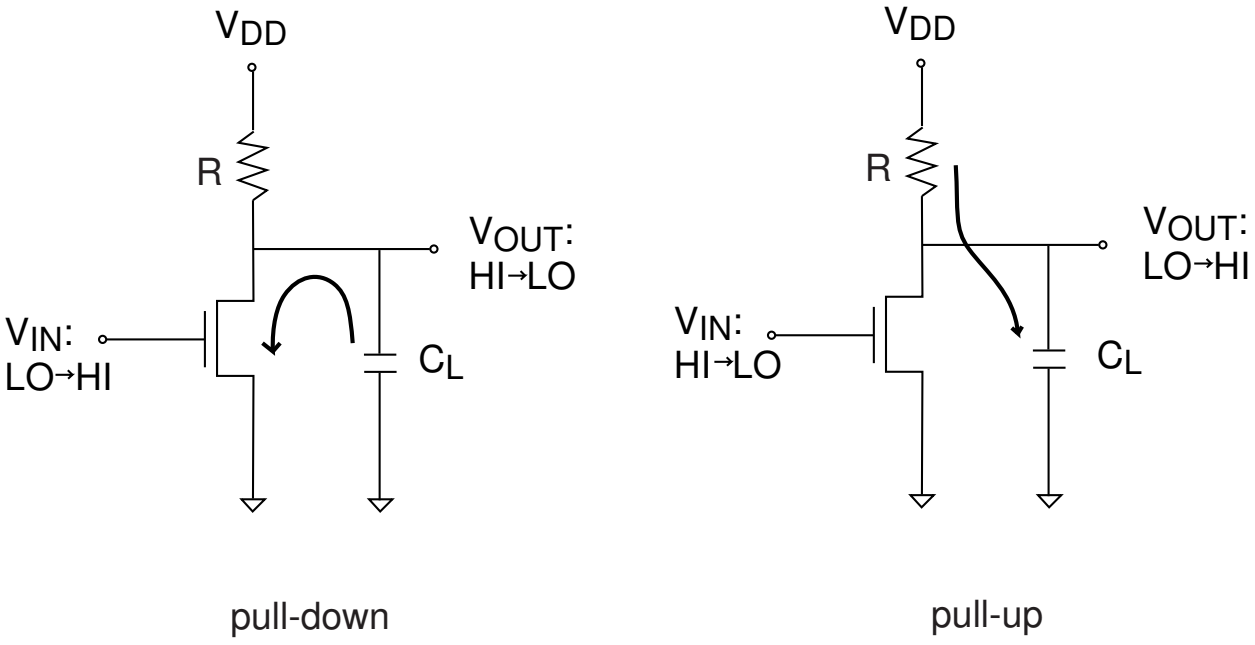
- NMOS inverter with resistor pull-up
  - –The inverter
- NMOS inverter with current-source pull-up
- Complementary MOS (CMOS) inverter
- Static analysis of CMOS inverter

Reading Assignment:
Howe and Sodini; Chapter 5, Section 5.4

1. NMOS inverter with resistor pull-up:

Dynamics

- C_L ***pull-down*** limited by current through transistor
  - [shall study this issue in detail with CMOS]
- C_L ***pull-up*** limited by resistor ($t_{PLH} \approx RC_L$)
- Pull-up slowest



1. NMOS inverter with resistor pull-up:

Inverter design issues

Noise margins $\uparrow \Rightarrow |A_v| \uparrow \Rightarrow$

- $R \uparrow \Rightarrow |RC_L| \uparrow \Rightarrow$ slow switching
- $g_m \uparrow \Rightarrow |W| \uparrow \Rightarrow$ big transistor
  - (slow switching at input)

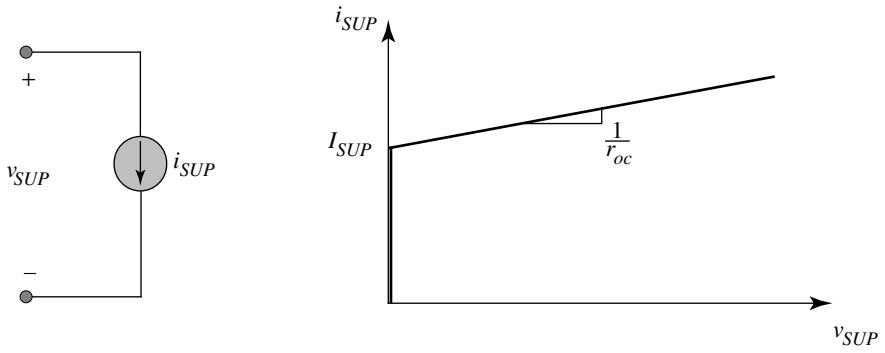
Trade-off between speed and noise margin.

During pull-up we need:

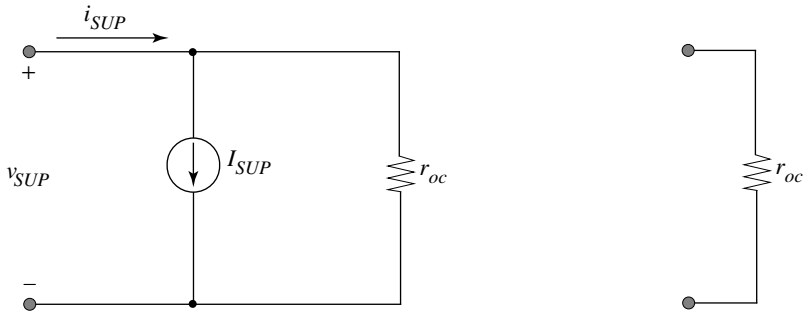
- High current for fast switching
- But also high incremental resistance for high noise margin.

2. NMOS inverter with current-source pull-up

I—V characteristics of current source:



Equivalent circuit models :

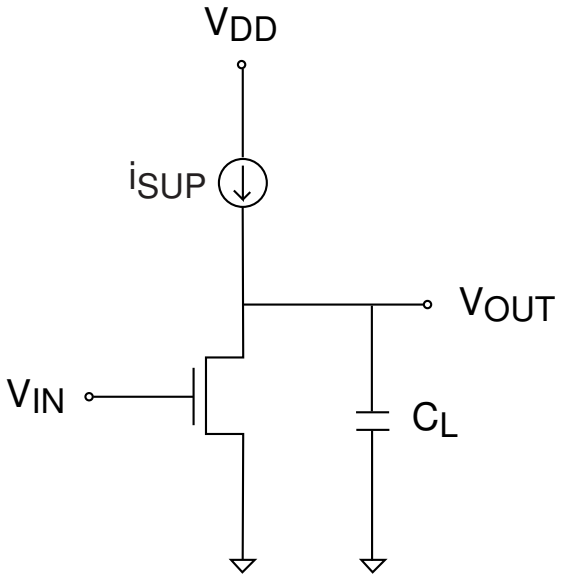


large-signal model small-signal model

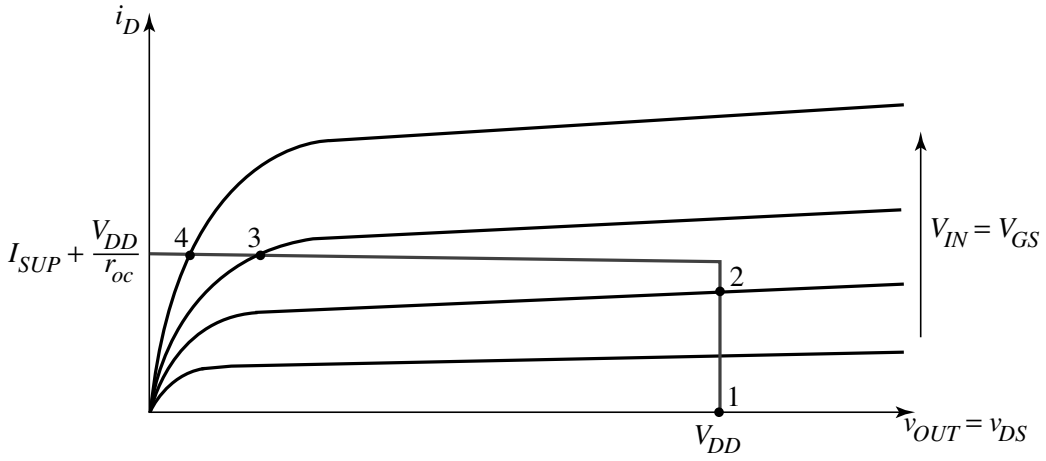
- High current throughout voltage range $v_{SUP} > 0$
- $i_{SUP} = 0$ for $v_{SUP} \leq 0$
- $i_{SUP} = I_{SUP} + v_{SUP}/ r_{oc}$ for $v_{SUP} > 0$
- High small-signal resistance $r_{oc.}$

NMOS inverter with current-source pull-up

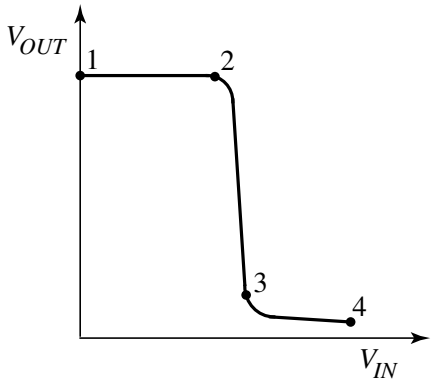
Static Characteristics



Inverter characteristics :



(a)

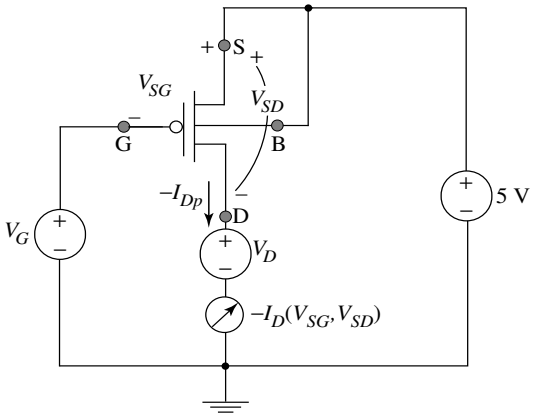


(b)

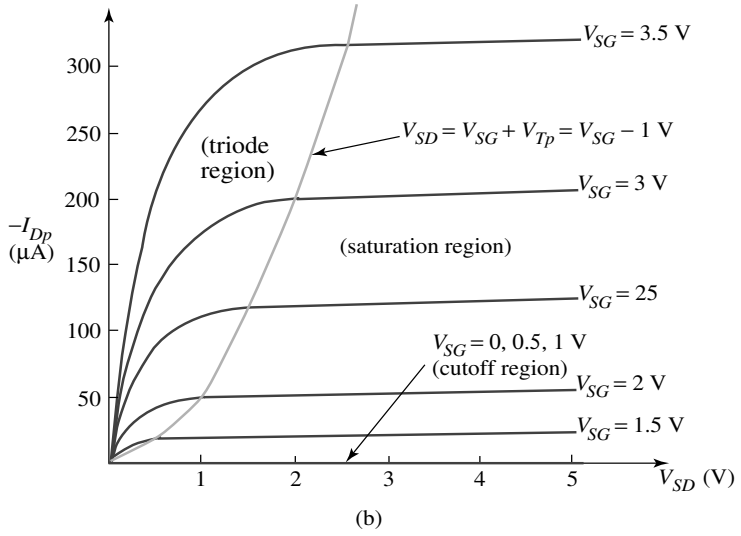
High $r_{oc} \Rightarrow$ high noise margins

PMOS as current-source pull-up

I—V characteristics of PMOS:



(a)



(b)

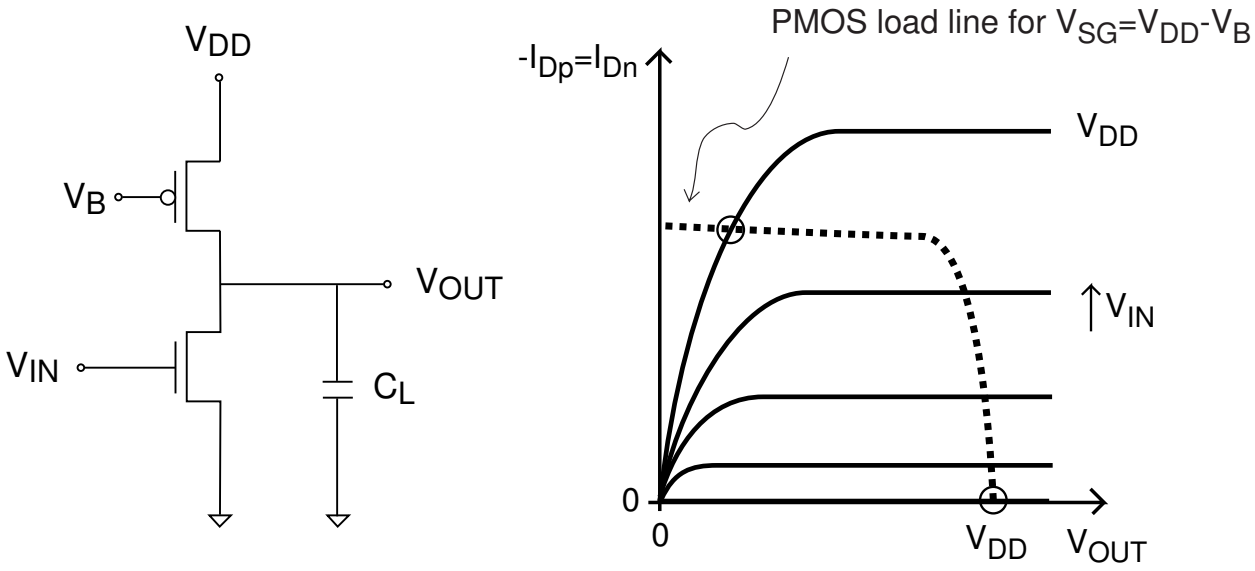
Note: enhancement-mode PMOS has $V_{Tp} < 0$.

In saturation:

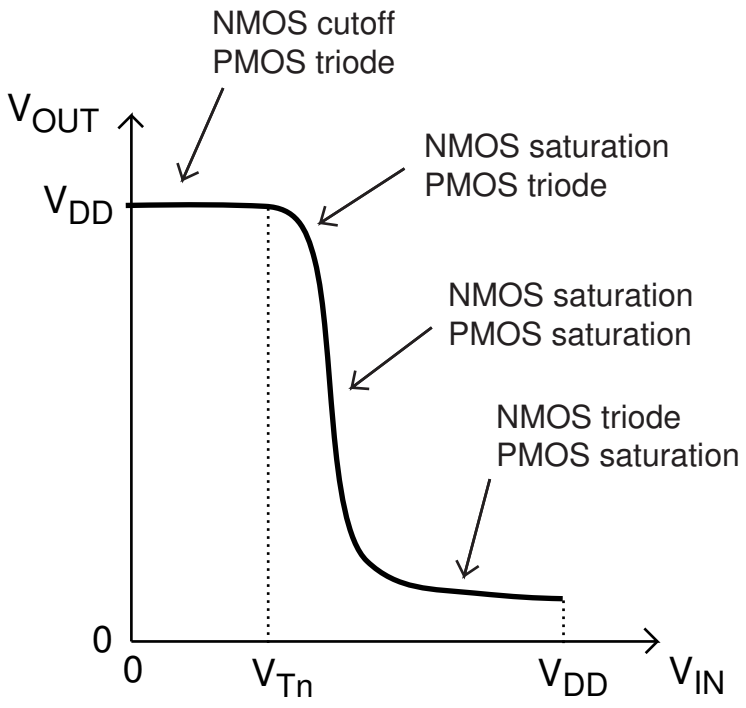
$$-I_{Dp} \propto \left(V_{SG} + V_{Tp}\right)^2$$

PMOS as current-source pull-up:

Circuit and load-line diagram of inverter with PMOS current source pull-up:



Inverter characteristics:



PMOS as current-source pull-up:

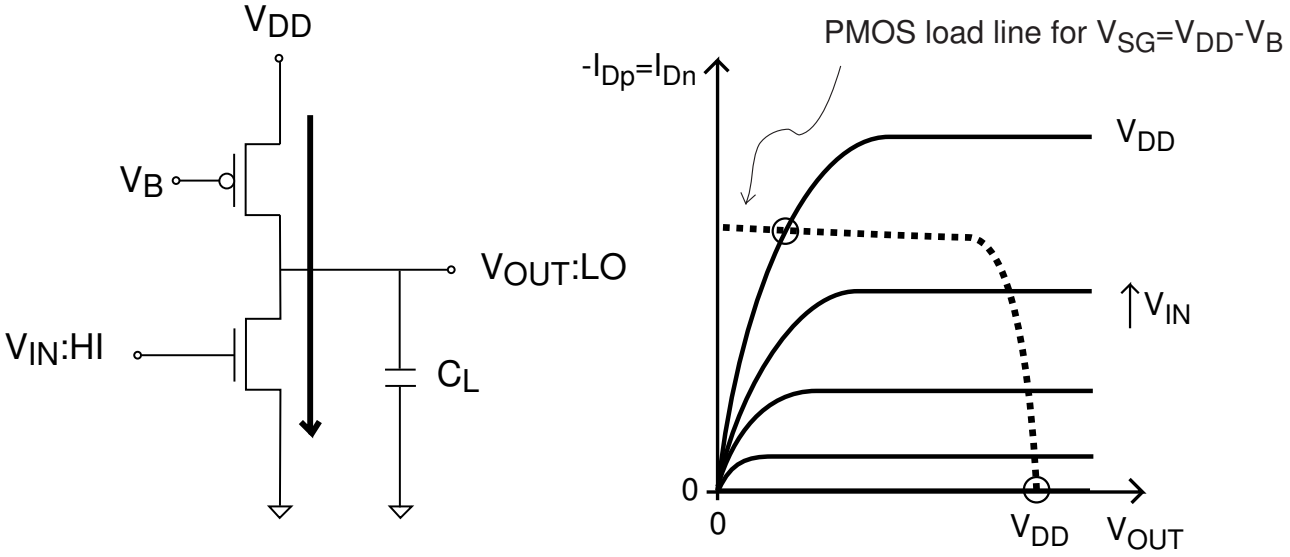
NMOS inverter with current-source pull-up allows high ***noise margin*** with ***fast switching***

- High Incremental resistance
- Constant charging current of load capacitance

But…

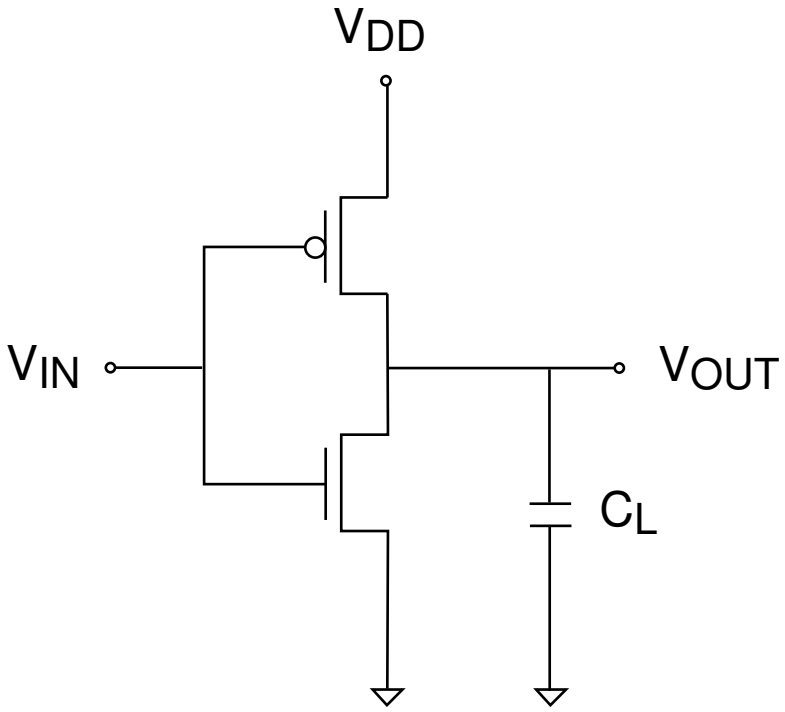
When $V_{IN} = V_{DD}$, there is a direct current path between supply and ground

$\Rightarrow$ power is consumed even if the inverter is idle.



3. Complementary MOS (CMOS) Inverter

Circuit schematic:



Basic Operation:

- $V_{IN} = 0 \Rightarrow V_{OUT} = V_{DD}$

  $V_{GSn} = 0 < V_{Tn} \Rightarrow$ **NMOS OFF**

  $V_{SGp} = V_{DD} > -V_{Tp} \Rightarrow$ **PMOS ON**

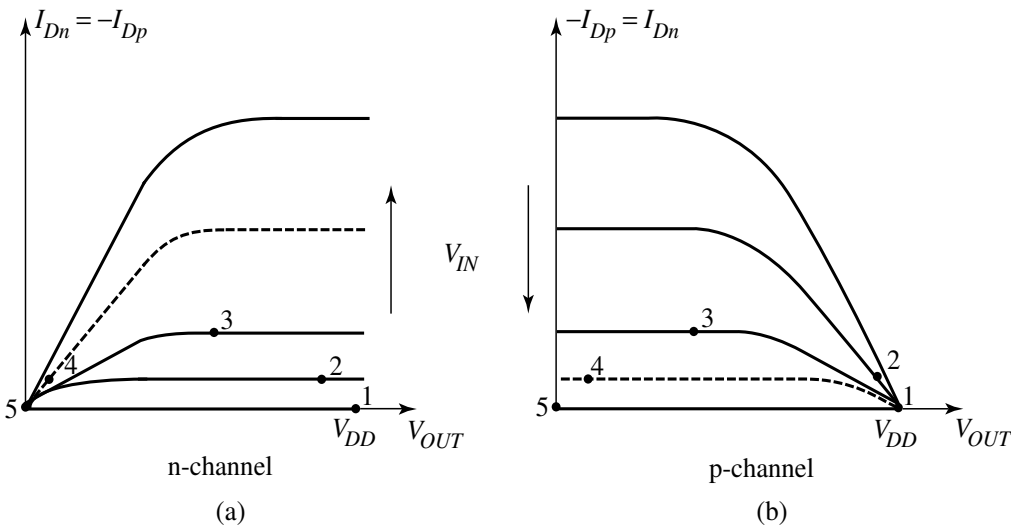
- $V_{IN} = V_{DD} \Rightarrow V_{OUT} = 0$

  $V_{GSn} = V_{DD} > V_{Tn} \Rightarrow$ **NMOS ON**

  $V_{SGp} = 0 < -V_{Tp} \Rightarrow$ **PMOS OFF**

CMOS Inverter (Contd.):

Output characteristics of both transistors:



Note:

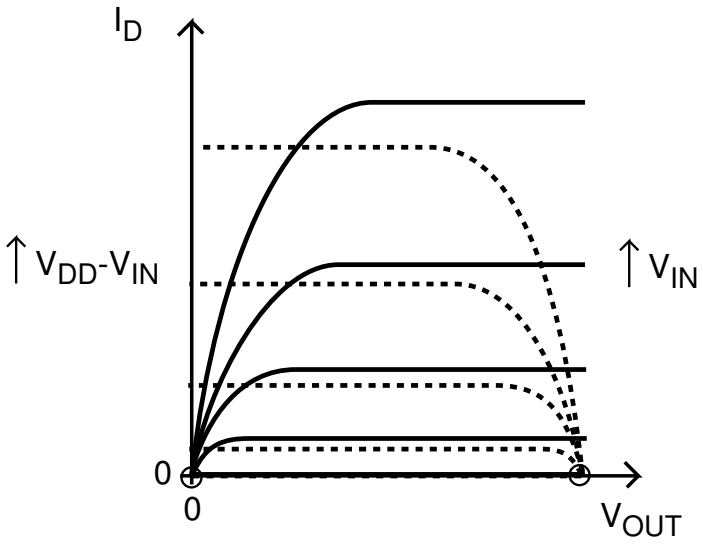
$V_{IN} = V_{GSn} = V_{DD} - V_{SGp} \Rightarrow V_{SGp} = V_{DD} - V_{IN}$

$V_{OUT} = V_{DSn} = V_{DD} - V_{SDp} \Rightarrow V_{SDp} = V_{DD} - V_{OUT}$

$I_{Dn} = -I_{Dp}$

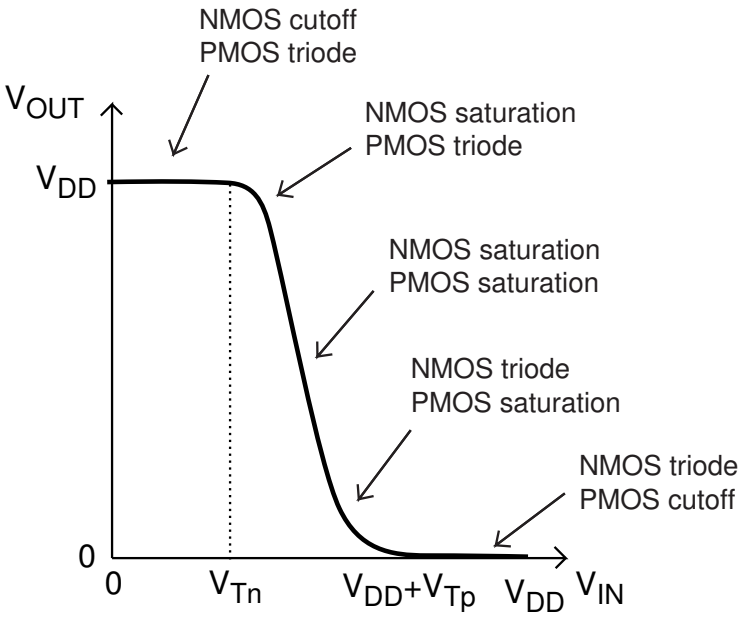
Combine into single diagram of I_D vs. V_{OUT} with V_{IN} as parameter

CMOS Inverter (Contd.):



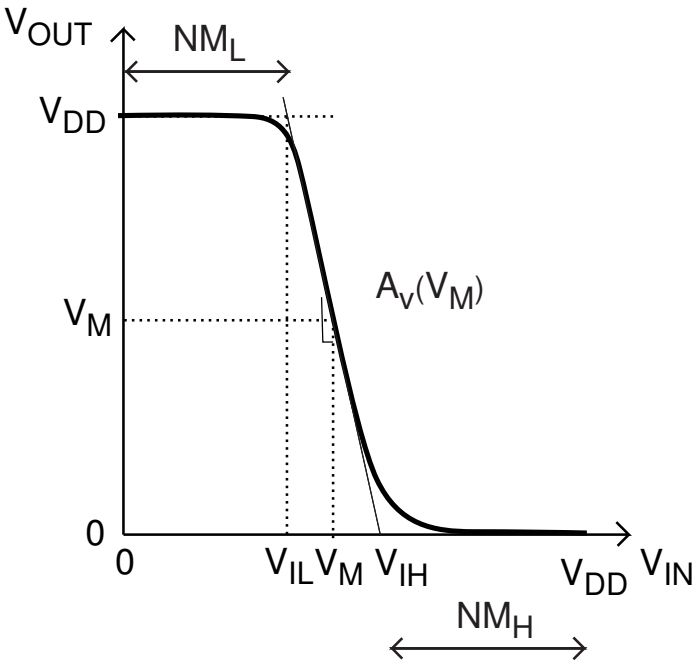
- *No current while idle in any logic state*

Inverter Characteristics:



- *"rail-to-rail" logic: logic levels are 0 and V_{DD}*
- *High $|A_v|$ around logic threshold*
  $\Rightarrow$ good noise margins

2. CMOS inverter: noise margins



- Calculate V_M
- Calculate $A_v(V_M)$
- Calculate NM_L and NM_H

Calculate V_M ($V_M = V_{IN} = V_{OUT}$)

At V_M both transistors are saturated:

$$I_{Dn} = \frac{W_n}{2L_n}\mu_n C_{ox}\left(V_M - V_{Tn}\right)^2$$

$$-I_{Dp} = \frac{W_p}{2L_p}\mu_p C_{ox}\left(V_{DD} - V_M + V_{Tp}\right)^2$$

CMOS inverter: noise margins (contd.)

Define:

$$k_n = \frac{W_n}{L_n}\mu_n C_{ox}; \qquad k_p = \frac{W_p}{L_p}\mu_p C_{ox}$$

Since :

$$I_{Dn} = -I_{Dp}$$

Then:

$$\frac{1}{2}k_n\left(V_M - V_{Tn}\right)^2 = \frac{1}{2}k_p\left(V_{DD} - V_M + V_{Tp}\right)^2$$

Solve for V_M:

$$V_M = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}\left(V_{DD} + V_{Tp}\right)}{1 + \sqrt{\frac{k_p}{k_n}}}$$

Usually, V_{Tn} and V_{Tp} fixed and $V_{Tn} = -V_{Tp}$
$\Rightarrow V_M$ engineered through k_p/k_n ratio.

CMOS inverter: noise margins (contd..)

- **Symmetric case**: $k_n = k_p$

$$V_M = \frac{V_{DD}}{2}$$

This implies:

$$\frac{k_p}{k_n} = 1 = \frac{\frac{W_p}{L_p}\mu_p C_{ox}}{\frac{W_n}{L_n}\mu_n C_{ox}} \approx \frac{\frac{W_p}{L_p}\mu_p}{\frac{W_n}{L_n}2\mu_p} \Rightarrow \frac{W_p}{L_p} \approx 2\frac{W_n}{L_n}$$

Since usually $L_p \approx L_n = L_{min} \Rightarrow W_p \approx 2W_n$

- **Asymmetric case**: $k_n >> k_p$, or $\frac{W_n}{L_n} >> \frac{W_p}{L_p}$

$$V_M \approx V_{Tn}$$

NMOS turns on as soon as V_{IN} goes above V_{Tn}.

- **Asymmetric case**: $k_n << k_p$, or $\frac{W_n}{L_n} << \frac{W_p}{L_p}$

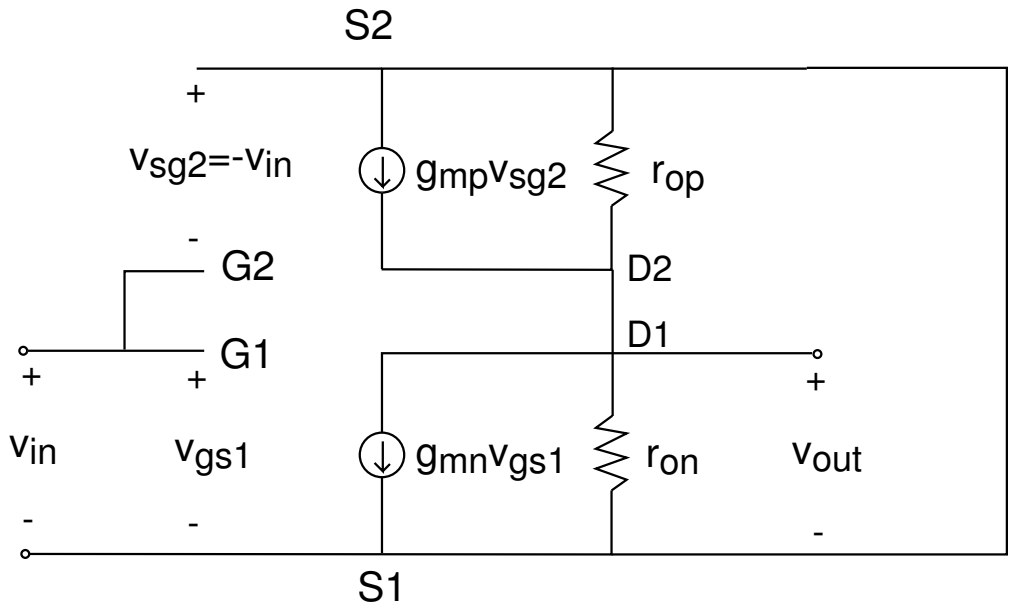
$$V_M \approx V_{DD} + V_{Tp}$$

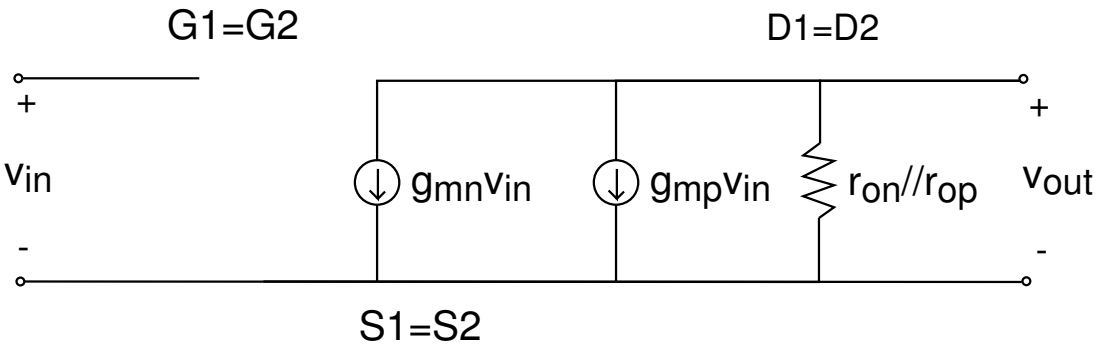
PMOS turns on as soon as V_{IN} goes below $V_{DD} + V_{Tp}$.

CMOS inverter: noise margins (contd…)

Calculate $A_v(V_M)$

- Small signal model:

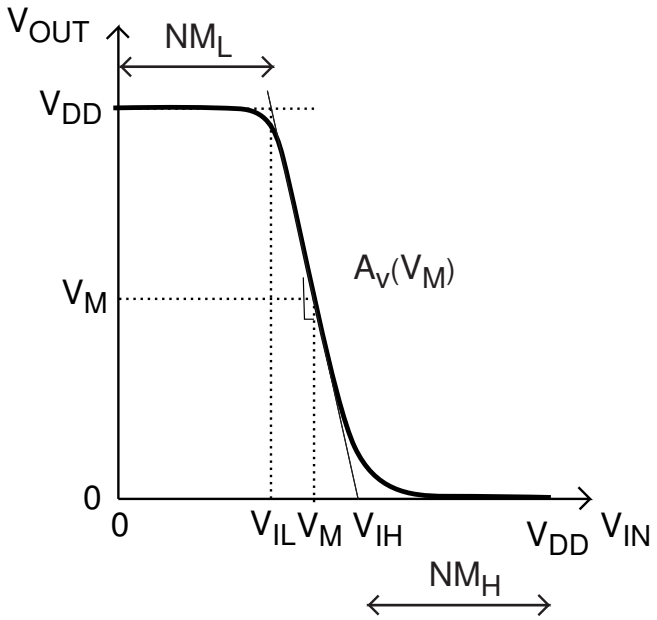




$$A_v = -(g_{mn} + g_{mp})(r_{on} // r_{op})$$

This can be rather large.

CMOS inverter: calculate noise margins (contd.)



- Noise-margin low, NM_L:

$$V_{IL} = V_M - \frac{V_{DD} - V_M}{|A_v|}$$

$$NM_L = V_{IL} - V_{OL} = V_{IL} = V_M - \frac{V_{DD} - V_M}{|A_v|}$$

- Noise-margin high, NM_H:

$$V_{IH} = V_M\left(1 + \frac{1}{|A_v|}\right)$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_M\left(1 + \frac{1}{|A_v|}\right)$$

What did we learn today?

Summary of Key Concepts

- In NMOS inverter with resistor pull-up, there is a trade-off between noise margin and speed
- Trade-off resolved using current source pull-up
  - **Use PMOS as current source**.
- In NMOS inverter with current-source pull-up: if V_{IN} = High, there is power consumption even if inverter is idling.
- Complementary MOS: **NMOS and PMOS switch-on alternatively**.
  - No current path between power supply and ground
  - No power consumption while idling
- Calculation of CMOS
  - V_M
  - Noise Margin

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