

## Lecture 13 - Digital Circuits (II)

### MOS INVERTER CIRCUITS

October 25, 2005

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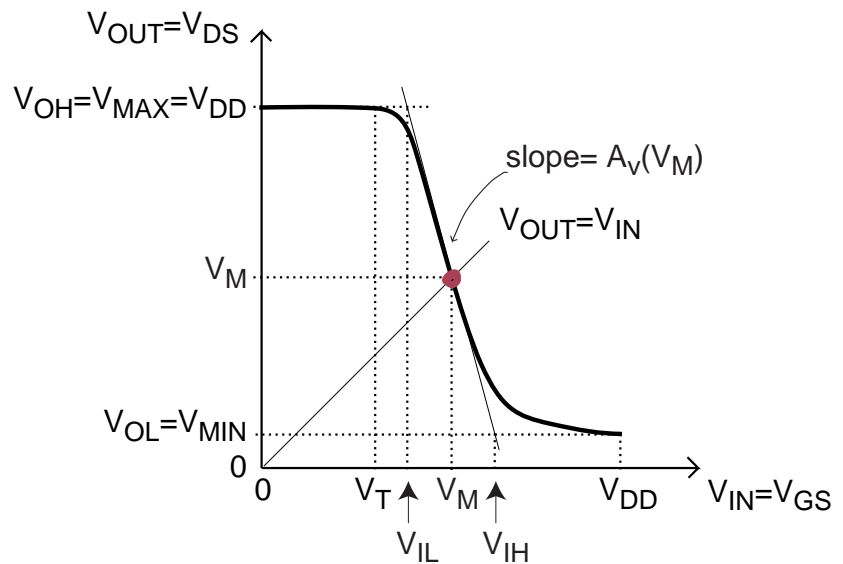
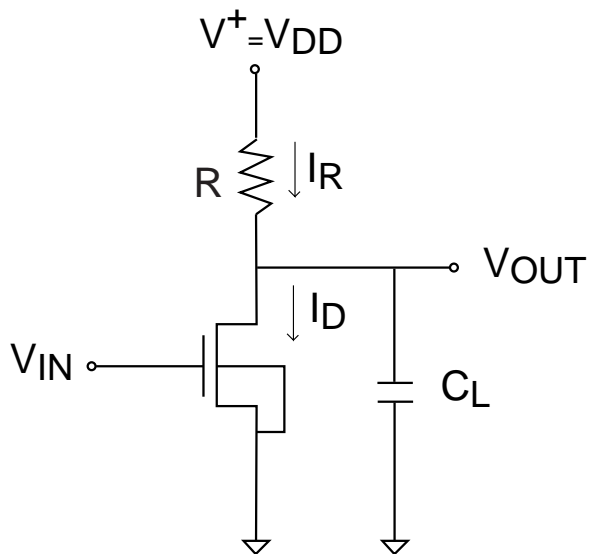
#### Reading assignment:

Howe and Sodini, Ch. 5, §5.3

## Key questions

- What are the key design trade-offs of the NMOS inverter with resistor pull-up?
- How can one improve upon these trade-offs?
- What is special about a CMOS inverter?

# 1. NMOS inverter with resistor pull-up (*cont.*)



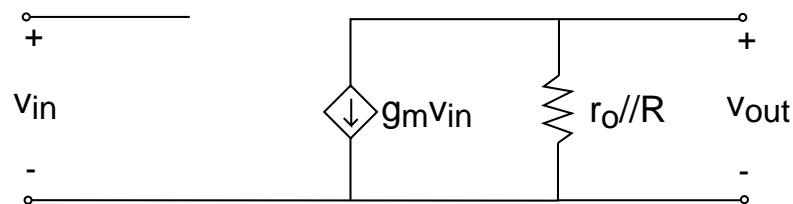
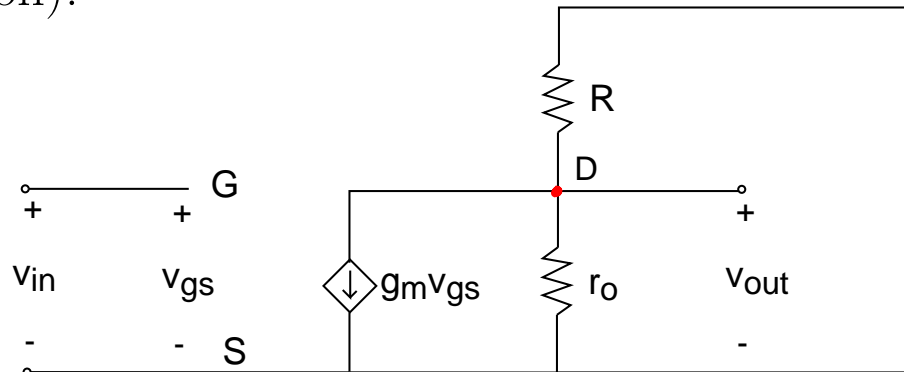
□ Noise margins:

$$NM_L = V_{IL} - V_{OL} = V_M - \frac{V_{MAX} - V_M}{|A_v(V_M)|} - V_{MIN}$$

$$NM_H = V_{OH} - V_{IH} = V_{MAX} - V_M \left(1 + \frac{1}{|A_v(V_M)|}\right) + \frac{V_{MIN}}{|A_v(V_M)|}$$

Need to compute  $|A_v(V_M)|$ .

Small-signal equivalent circuit model at  $V_M$  (transistor in saturation):



$$v_{out} = -g_m v_{in} (r_o // R)$$

Then:

$$A_v = \frac{v_{out}}{v_{in}} = -g_m (r_o // R) \simeq -g_m R$$

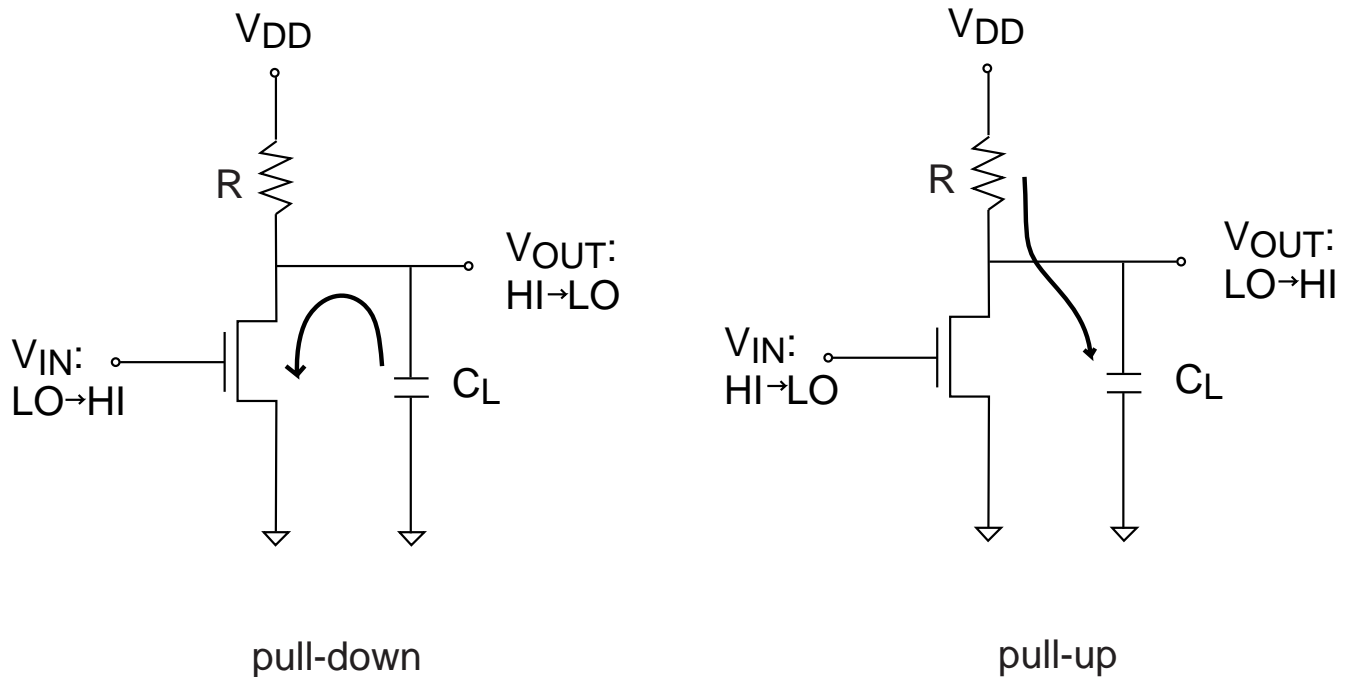
Then:

$$|A_v(V_M)| = g_m(V_M) R$$

From here, get  $NM_L$  and  $NM_H$  using above formulae.

## □ Dynamics

- $C_L$  pull-down limited by current through transistor [will study in detail with CMOS]
- $C_L$  pull-up limited by resistor ( $t_{PLH} \sim RC_L$ )
- pull-up slowest



□ Inverter design issues:

noise margins  $\uparrow \Rightarrow |A_v| \uparrow \Rightarrow$

- $R \uparrow \Rightarrow RC_L \uparrow \Rightarrow$  slow switching
- $g_m \uparrow \Rightarrow W \uparrow \Rightarrow$  big transistor  
(slow switching at input)

*Trade-off between speed and noise margin.*

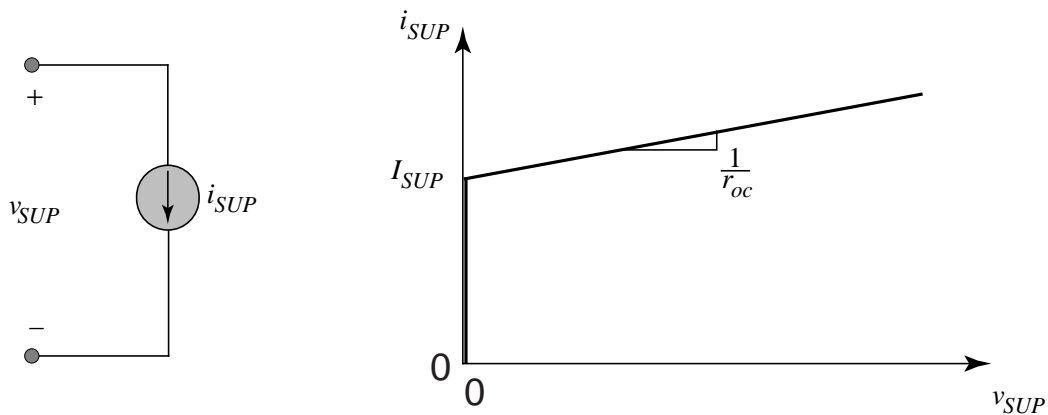
During pull-up, need:

- high current for fast switching,
- but also high resistance for high noise margin.

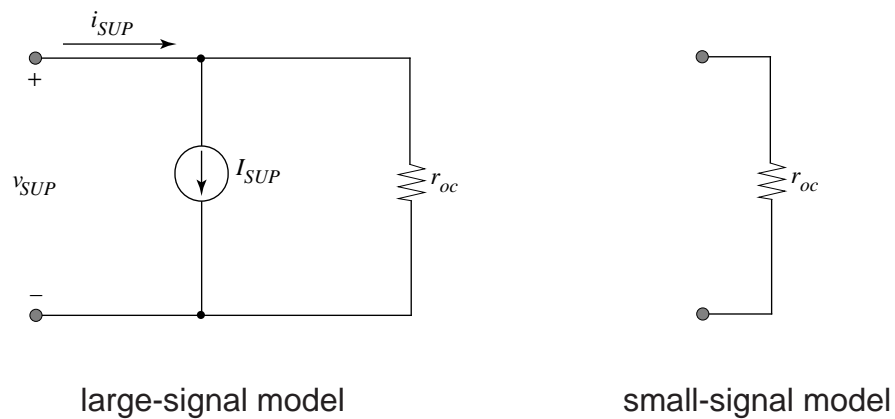
$\Rightarrow$  use *current source* as pull-up.

## 2. NMOS inverter with current-source pull-up

I-V characteristics of current source:

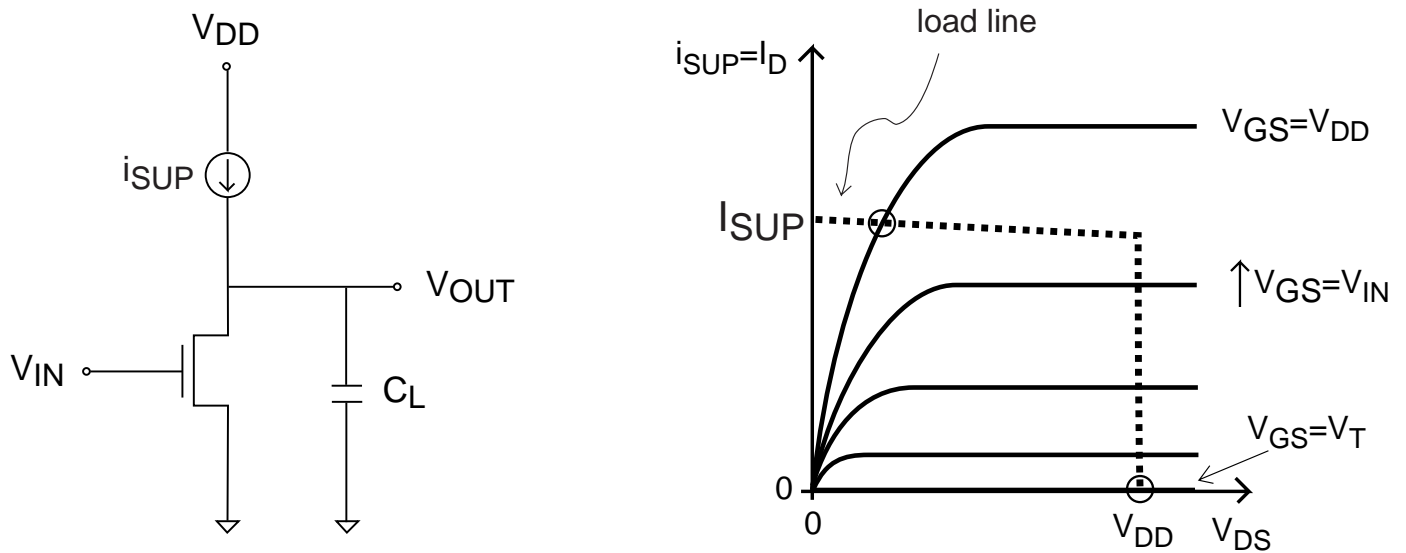


Equivalent circuit models:

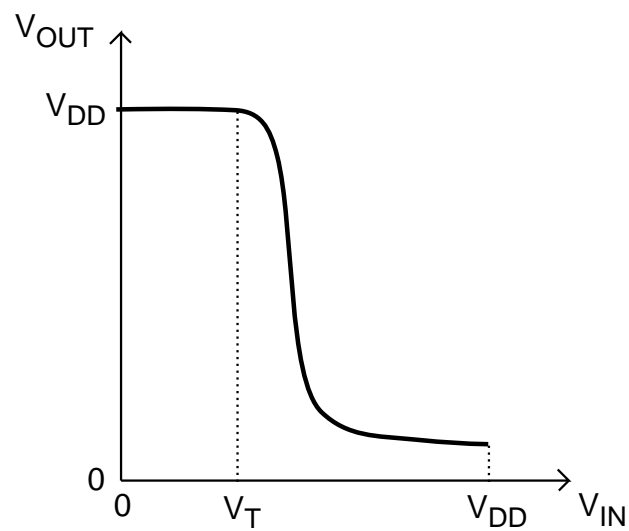


- high current throughout voltage range:  $i_{SUP} \simeq I_{SUP}$
- high small-signal resistance,  $r_{oc}$ .

## NMOS inverter with current-source pull-up:



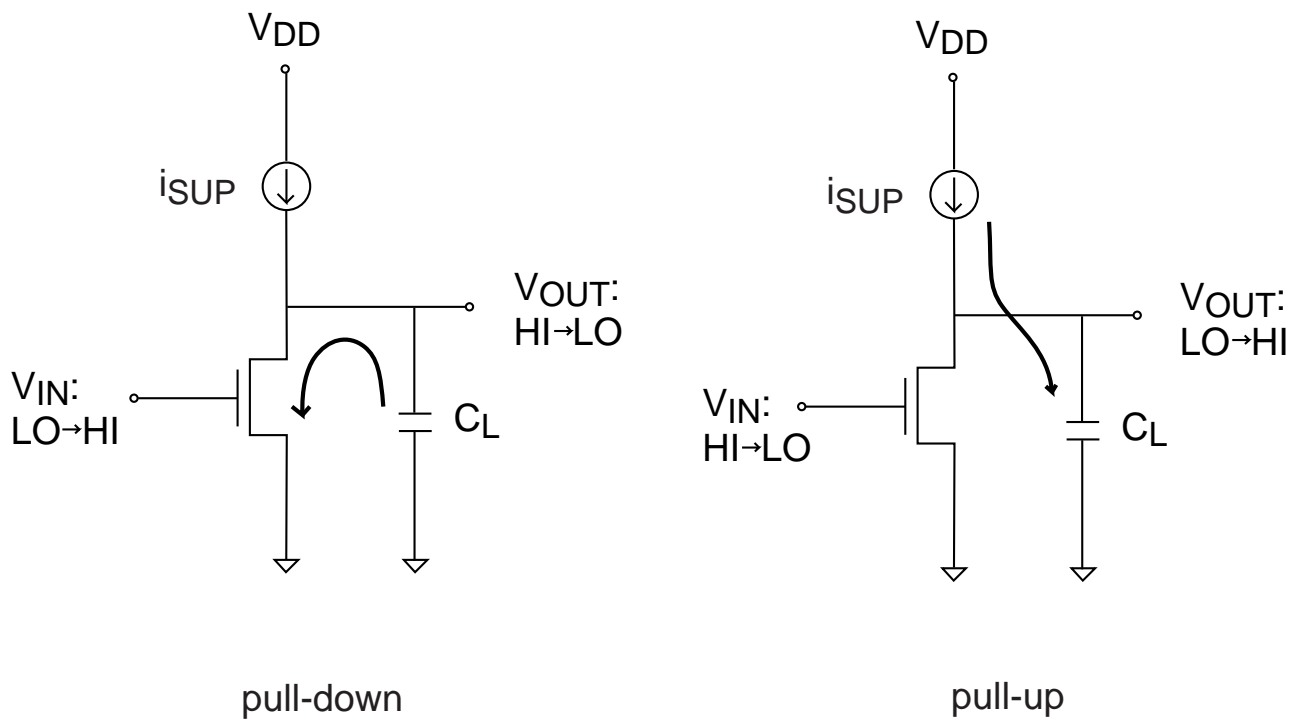
## Transfer characteristics:



High  $r_{oc} \Rightarrow$  high noise margin



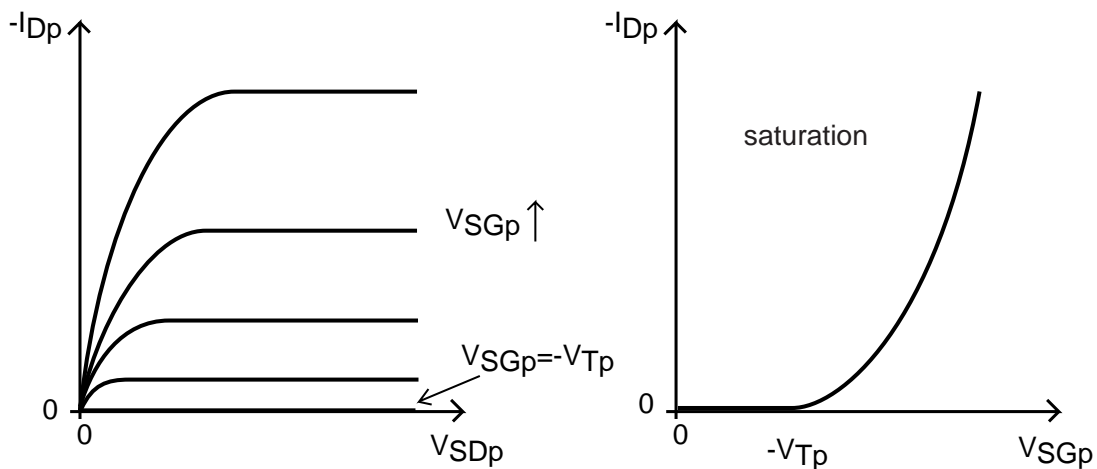
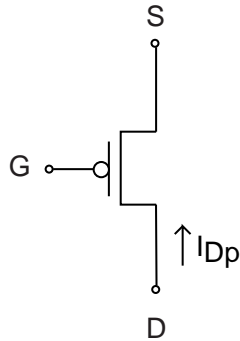
Dynamics:



Faster pull-up because capacitor charged at constant current.

## □ PMOS as current-source pull-up

I-V characteristics of PMOS:

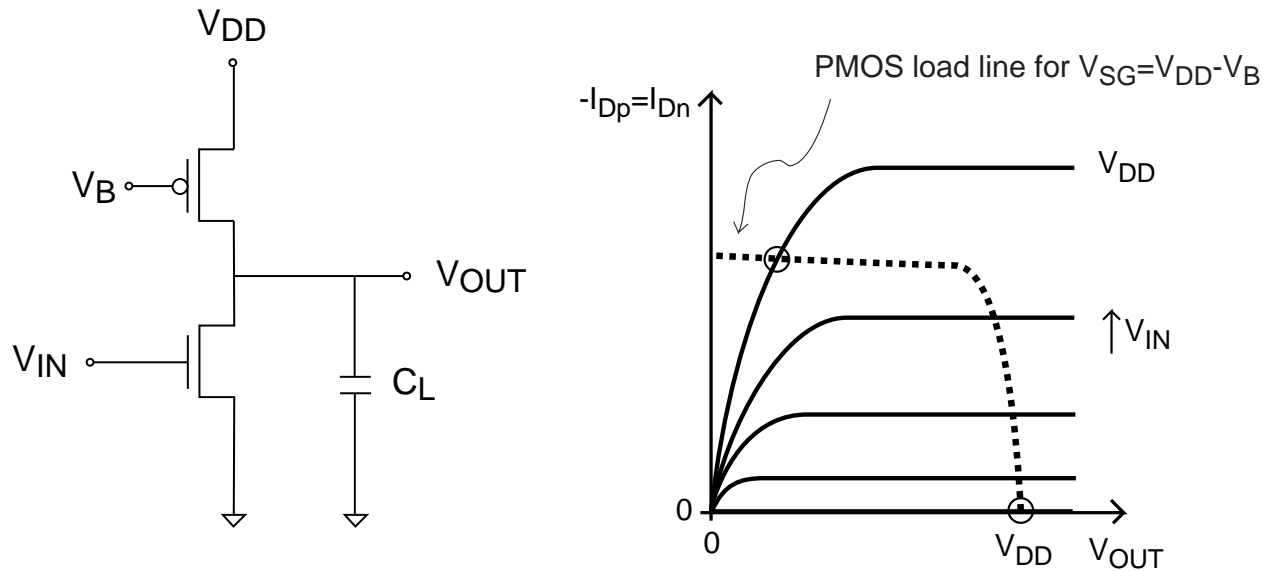


Note: enhancement-mode PMOS has  $V_{Tp} < 0$ .

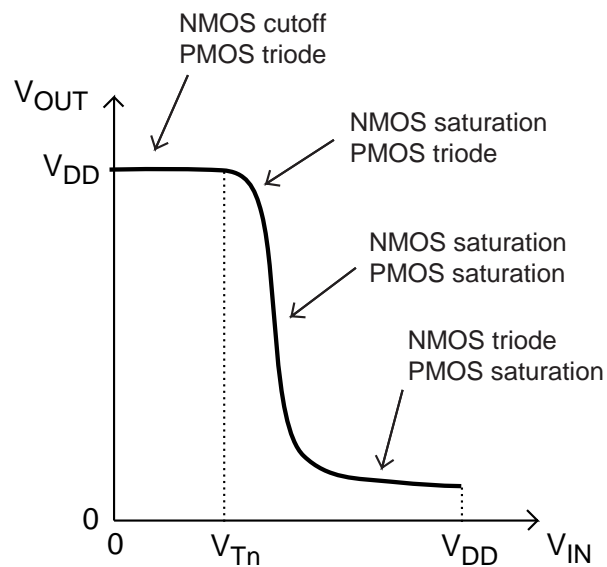
In saturation:

$$-I_{Dp} \propto (V_{SG} + V_{Tp})^2$$

Circuit and load-line diagram of inverter with PMOS current source pull-up:



Transfer function:



Noise margin:

- compute  $V_M = V_{IN} = V_{OUT}$
- compute  $|A_v(V_M)|$

At  $V_M$  both transistors saturated:

$$I_{Dn} = \frac{W_n}{2L_n} \mu_n C_{ox} (V_M - V_{Tn})^2$$

$$-I_{Dp} = \frac{W_p}{2L_p} \mu_p C_{ox} (V_{DD} - V_B + V_{Tp})^2$$

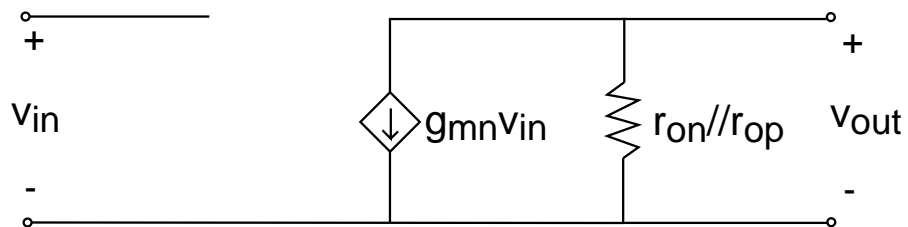
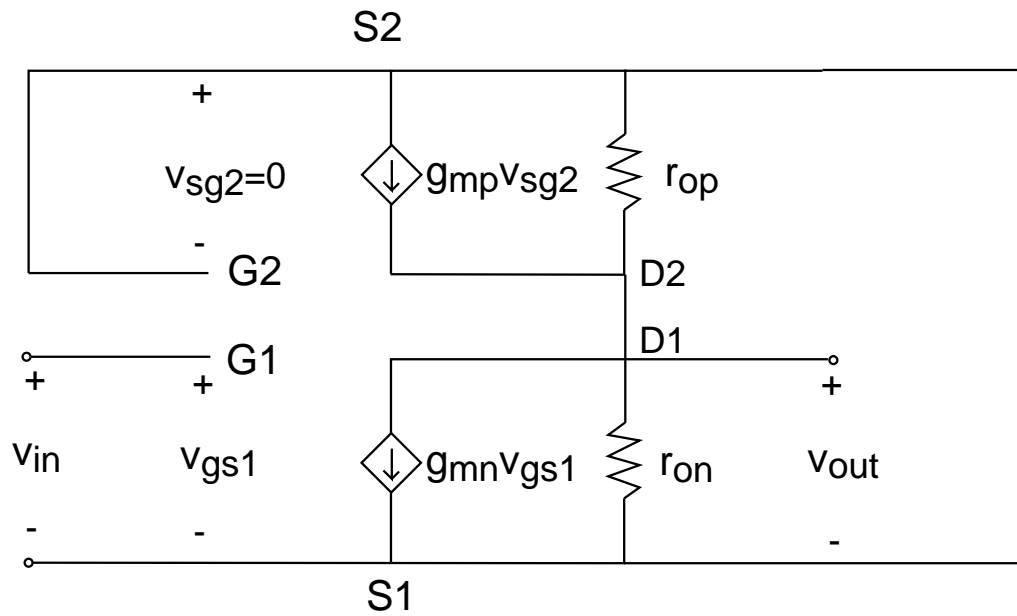
And:

$$I_{Dn} = -I_{Dp}$$

Then:

$$V_M = V_{Tn} + \sqrt{\frac{\mu_p \frac{W_p}{L_p}}{\mu_n \frac{W_n}{L_n}}} (V_{DD} - V_B + V_{Tp})$$

Small-signal equivalent circuit model at  $V_M$ :

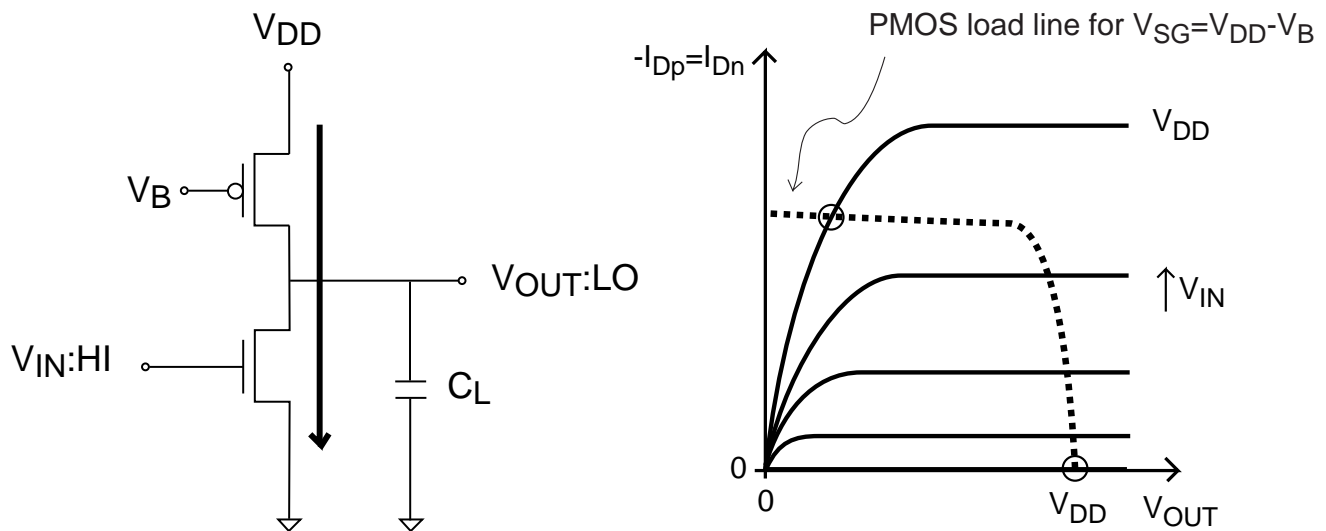


$$A_v = -g_{mn}(r_{on} // r_{op})$$

NMOS inverter with current-source pull-up allows fast switching with high noise margins.

But... when  $V_{IN} = V_{DD}$ , there is a direct current path between supply and ground

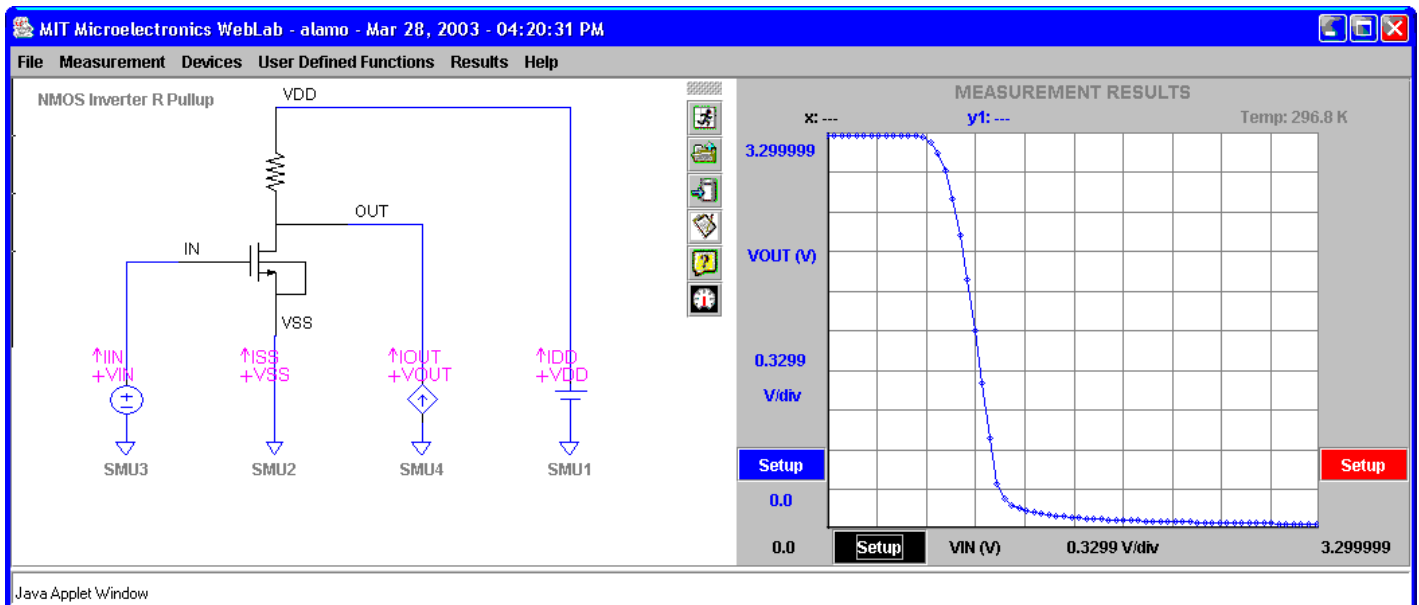
$\Rightarrow$  power consumption even if inverter is idling.



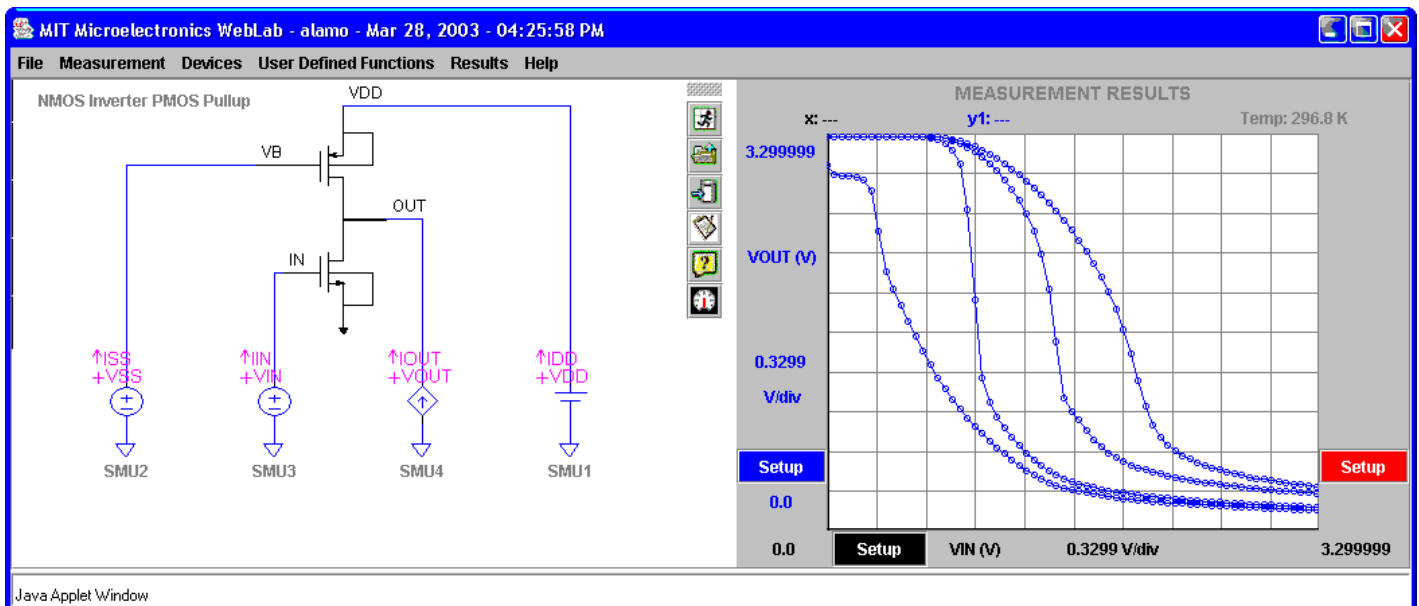
Would like to have current source that is *itself* switchable, *i.e.*, it shuts off when input is high  $\Rightarrow$  CMOS!

## Screen shots of NMOS inverter transfer characteristics:

- NMOS inverter with resistor pull-up

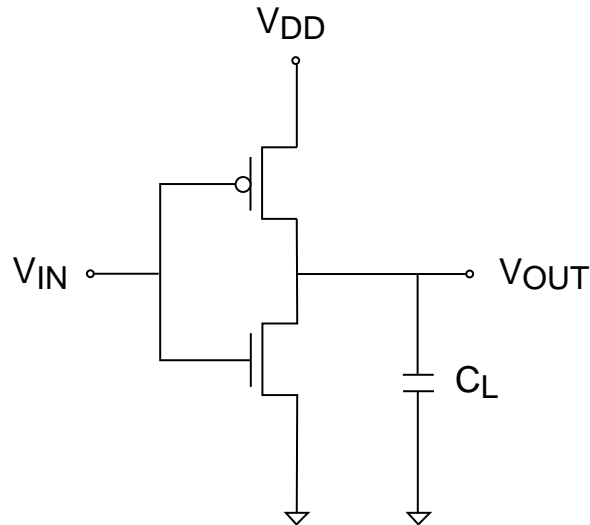


- NMOS inverter with current source pull-up



### 3. Complementary MOS (CMOS) Inverter

Circuit schematic:



Basic operation:

- $V_{IN} = 0 \Rightarrow V_{OUT} = V_{DD}$

$$V_{GSn} = 0 < V_{Tn} \Rightarrow \text{NMOS OFF}$$

$$V_{SGp} = V_{DD} > -V_{Tp} \Rightarrow \text{PMOS ON}$$

- $V_{IN} = V_{DD} \Rightarrow V_{OUT} = 0$

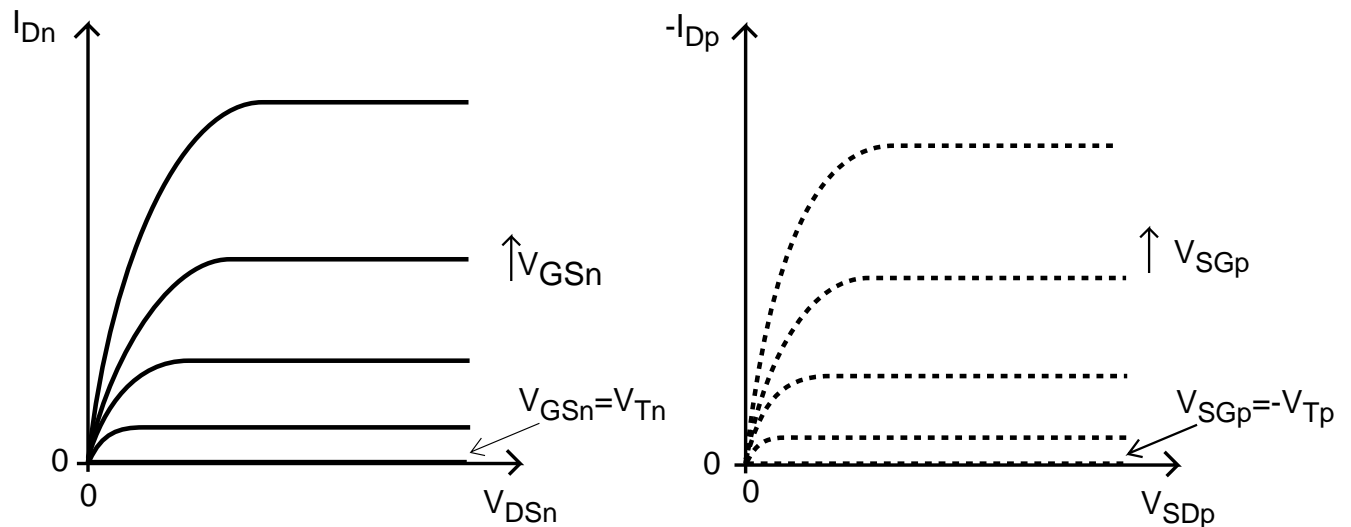
$$V_{GSn} = V_{DD} > V_{Tn} \Rightarrow \text{NMOS ON}$$

$$V_{SGp} = 0 < -V_{Tp} \Rightarrow \text{PMOS OFF}$$

No power consumption while idling in any logic state.



Output characteristics of both transistors:



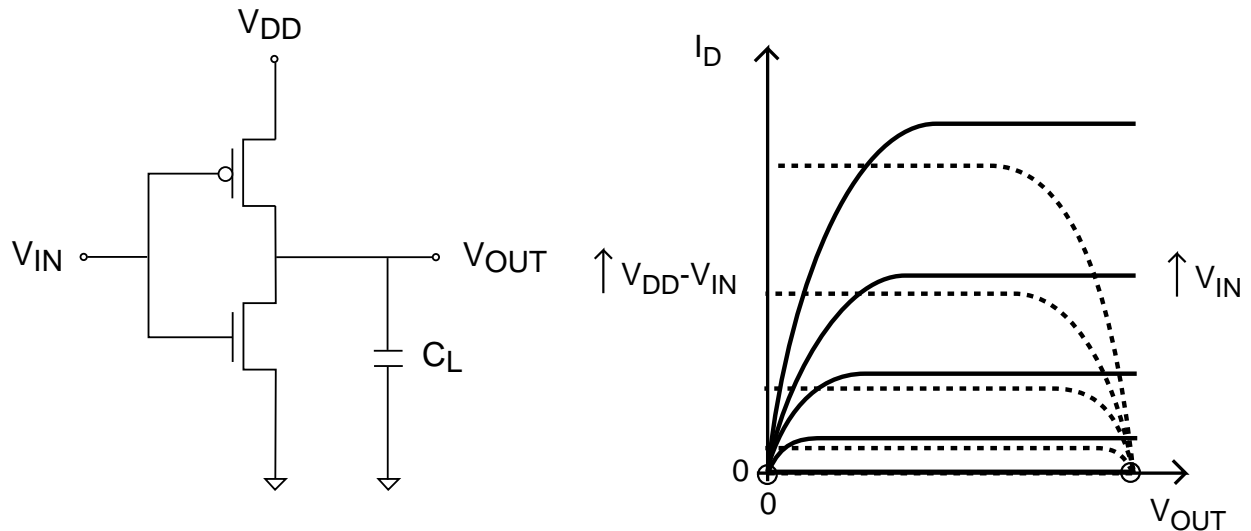
Note:

$$V_{IN} = V_{GSn} = V_{DD} - V_{SGp} \Rightarrow V_{SGp} = V_{DD} - V_{IN}$$

$$V_{OUT} = V_{DSn} = V_{DD} - V_{SDp} \Rightarrow V_{SDp} = V_{DD} - V_{OUT}$$

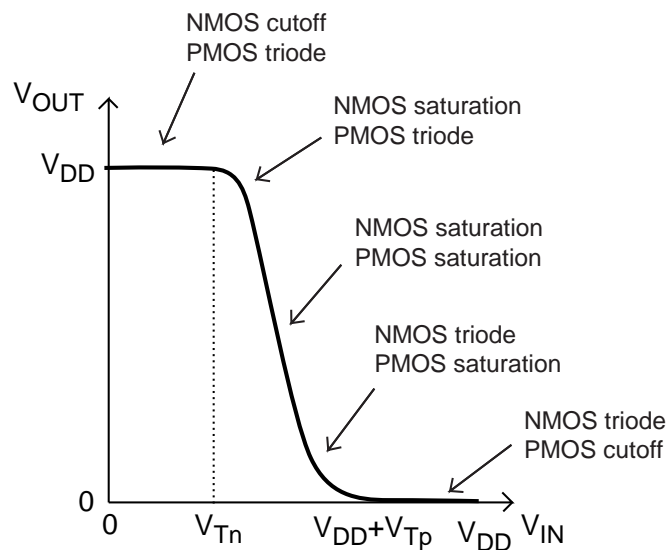
$$I_{Dn} = -I_{Dp}$$

Combine into single diagram of  $I_D$  vs.  $V_{OUT}$  with  $V_{IN}$  as parameter.



★ *no current while idling in any logic state.*

Transfer function:



★ *"rail-to-rail" logic: logic levels are 0 and  $V_{DD}$*

★ *high  $|A_v|$  around logic threshold  $\Rightarrow$  good noise margins*



## Key conclusions

- In NMOS inverter with resistor pull-up: trade-off between noise margin and speed.
- Trade-off resolved using current-source pull-up: use PMOS as current source.
- In NMOS inverter with current-source pull-up: if  $V_{IN} = HI$ , power consumption even if inverter is idling.
- Complementary MOS: NMOS and PMOS switch alternatively  $\Rightarrow$ 
  - no power consumption while idling
  - "rail-to-rail" logic: logic levels are 0 and  $V_{DD}$
  - high  $|A_v|$  around logic threshold  $\Rightarrow$  good noise margins